REMARKS

Claims 1-20 and 22-29 are pending in the present application.

This Amendment is in response to the Office Action mailed April 9, 2002. In the Office Action, the Examiner objected to the title, Abstract of the Disclosure and rejected claims 1-20 and 22-29 under 35 U.S.C. §102(a)(b)(e). Applicant has amended the title and the abstract. Reconsideration in light of the amendments and remarks made herein is respectfully requested.

I. TITLE

In the Office Action, the Examiner objected to the title. In particular, the Examiner stated that the title of the invention is neither descriptive nor precise. In response, Applicant has amended the title to change to SELECTING DESIGN POINTS ON PARAMETER FUNCTIONS HAVING FIRST SUM OF CONSTRAINT SET AND SECOND SUM OF OPTIMIZING SET TO IMPROVE SECOND SUM WITHIN DESGIN CONSTRAINTS.

Therefore, Applicant respectfully requests the objection to the title be withdrawn.

II. SPECIFICATION

The Examiner objected to the Abstract. In response, Applicant has amended the Abstract accordingly. Therefore, Applicant respectfully requests the objection be withdrawn.

III. REJECTION UNDER 35 U.S.C. §102(A)(B)(E)

In the Office Action, the Examiner rejected Claims 1-20 and 22-29 under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 5,838,947 issued to Sarin ("Sarin") or U.S. Patent No. 5, 880,967 issued to Jyu et al. ("Jyu") or United States Patent No. 5,666,2888 issued to Jones et al. ("Jones") or U.S. Patent No. 5,835,380 issued to Roething ("Roething"). The Examiner also rejected Claims 1-20 and 22-29 under 35 U.S.C. § 102(a) as anticipated by Roething, and rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,619,420 issued to Breid ("Breid") and Applicant's own admittance (AOA) of the use of integrated commercial packages of Pathmill, Powermill, AMPS and ISPICE, iVGEN and ISPEC2. Applicant respectfully traverses the rejections for the following reasons.

Applicant reiterates the arguments set forth in the previously filed Response to the Office Action.

Sarin discloses a modeling, characterization and simulation of integrated circuit power behavior. Sarin merely discloses a method to simulate power behavior of digital VLSI MOS circuit at the gate level (Sarin, col. 2, lines 14-16). For each state-vector, power consumption measurements are carried out for different conditions of input ramp and output load (Sarin, col. 2, lines 22-24). A power dissipation model is used to predict power behavior (Sarin, col. 9, lines 23-36).

Jyu discloses a minimization of circuit delay and power through transistor sizing using an autosizing engine. Jyu discloses design goals commands including a requirement mode. In requirement mode, two requirement parameters may be specified: delay and power. If one requirement is specified, the engine will first satisfy the specified requirement and then minimize the other (Jyu, col. 10, lines 56-62). The autosizing engine performs initial search and select by simulating a circuit retrieved from netlist files (Jyu, col. 13, lines 26-37). Then, the engine generates user-specified scaling and changing circuits for power simulation and delay analysis (Jyu, col. 14, lines 53-69). The engine merely sizes up and down a transistor.

Jones discloses a method and apparatus for designing an integrated circuit. Jones discloses providing a behavioral model and an initial library of logic cells to a design synthesis tool (Jones, col. 3, lines 30-33). Cell strengths are altered by altering specific sizes of transistors in the gate schematic net list (Jones, col. 3, lines 41-42). The size alteration is used to achieve speed path constraints while minimizing area or power impact (Jones, col. 3, lines 42-43). Then, a new hybrid library must be generated taking into account the changes made by these optimizations (Jones, col. 3, lines 61-63).

Roethig discloses a simulation based extractor or expected waveforms for gate-level power analysis tool. Roethig discloses performing a simulation and then calculating power information from a database (Roethig, col. 4, lines 47-50). A power analysis tool includes a power calculator that converts average current, propagation delay, and intrinsic delay into positive and negative load currents for a cell (Roethig, col. 3, lines 10-13)

Breid discloses a semiconductor cell having a variable transistor width. A cell library definition includes a transistor width input variable which allows transistors in the cell to be sized during the layout process to eliminate timing violations and to minimize power consumption (Breid, col. 3, lines 54-59)

Sarin, Jyu, Jones, Roethig, and Breid, taken alone or in any combination, do not disclose, either expressly or inherently, suggest, or render obvious: (1) selecting initial design points having a first sum of the constraint set and a second sum of the optimizing set, (2) selecting the new design points such that the second sum is improved within the design constraints, and (3) selecting a first technology if the first improved optimizing parameter is better than the second improved optimizing parameter, and else selecting a second technology.

To anticipate a claim, the reference must teach every element of the claim. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Vergegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ...claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). Since the Examiner failed to show that Sarin, Jyu, Jones, Roethig, and Breid teaches or discloses any one of the above elements, the rejection under 35 U.S.C. §102 is improper.

In the Office Action, the Examiner stated that "Sarin and Jyu et al. and Roethig and Breid explicitly teach a constraint parameter set that is the propagation delay and an optimizing parameter set that is the power consumption." However, even assuming that this is true, none of the cited prior art references teach "selecting initial design points on the parameter functions having a first sum of the constraint set and a second sum of the optimizing set such that the first sum satisfies the design constraints."

The Examiner stated that Applicant is merely summing the sets of data to see if it meets and/or improves the design. However, none of the cited prior art references teach or suggest a parameter function having a first sum of the constraint set and a second sum of the optimizing set.

The Examiner further stated that Applicant's arguments amount to a general allegation that the claim define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. However, it is the Examiner who made a general allegation without specifically pointing out the column number and the line number of each of the cited references that teach: (1) first sum of constraint set, (2) second sum of optimizing set, (3) selecting initial design points such that first sum satisfies the design constraints, (4) selecting new design points such that the second sum is improved within the

design constraints, (5) selecting the first technology if the first improved optimizing parameter is better than the second improved optimizing parameter, else selecting the second technology.

Where a claim is refused for any reason relating to the merits thereof it should be "rejected" and the ground of rejection fully and clearly stated. See MPEP 707.07(d). Where the applicant traverses an objection, the Examiner should, if he or she repeats the rejection, take note of the applicant's argument and answer the substance of it. See MPEP 707.07(f). An omnibus rejection of the claim "on the reference and for reasons of record" is stereotyped and usually not informative and should therefore be avoided. See MPEP 707.07(d). It is important for an examiner to properly communicate the basis for a rejection so that the issues can be identified early and the applicant can be given fair opportunity to reply. See MPEP 706.02(j).

The Examiner should set forth in the Office Action the relevant teachings of the prior art relied upon, preferably with reference to the relevant column or page number(s) and line number(s) where appropriate. See MPEP 706.02(j). The goal of examination is to clearly articulate any rejection early in the prosecution process so that the applicant has the opportunity to provide evidence of a patentability and otherwise reply completely at the earliest opportunity. See MPEP 706.

The Examiner repeated the rejection without taking note of the Applicant's arguments and without answering the substance of Applicant's arguments as presented in the response previously filed. The MPEP requires that the Examiner's action will be complete as to all matters. 37 CRF 1.104; MPEP 707.07.

Therefore, Applicant believes that independent claims 1-20 and 22-29 and their respective dependent claims are distinguishable over the cited prior art references. Accordingly, Applicant respectfully requests the rejections under 35 U.S.C. §102(a)(b)(e) be withdrawn.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE TITLE

Please delete the Title of the Application and insert the following in lieu thereof:

--SELECTING DESIGN POINTS ON PARAMETER FUNCTIONS HAVING FIRST SUM OF CONSTRAINT SET AND SECOND SUM OF OPTIMIZING SET TO IMPROVE SECOND SUM WITHIN DESIGN CONSTRAINTS--

IN THE ABSTRACT

The Abstract of the Disclosure has been amended as follows:

--In one embodiment of the invention, parameter functions for a plurality of circuits in a subsystem are created. The subsystem has design constraints. Each one of the parameter functions corresponds to each one of the circuits. The parameter functions represent a relationship among design parameters of the subsystem. The design parameters include constraint and optimizing sets. Initial design points are selected on the parameter functions having a first sum of the constraint set and a second sum of the optimizing set such that the first sum satisfies the design constraints. New design points are selected on the parameter functions such that the second sum is improved within the design constraints.--

IN THE CLAIMS

No changes have been made to the claims.

CONCLUSION

In view of the amendments and remarks made above, it is respectfully submitted that the pending claims are in condition for allowance, and such action is respectfully solicited.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on: June 12, 2002.

Barbara Hayashi